ADC SINGLE SOCKET TESTER

REGISTER MAP

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| --- | --- | --- | --- | --- |
| **ADDRESS** | **NAME** | **R/W** | **BIT** | **FUNCTION** |
| 0 | SYS\_RESET | W | 0 | System reset (AUTO CLEARS) |
| 0 | REG\_RESET | W | 1 | Register reset -- clears only the Io registers (AUTO CLEARS) |
| 1 | ADC\_RESET | W | 0 | ADC ASIC reset (AUTO CLEARS) |
| 1 | SOFT\_ADC\_RESET | W | 2 | Soft ADC reset (AUTO CLEARS) |
| 2 | WRITE\_ADC\_ASIC\_SPI | W | 0 | Write ADC ASIC SPI (AUTO CLEARS) |
| 3 | TST\_PATT\_EN | R/W | 0 | EN ADC test pattern |
| 3 | TST\_PATT | R/W | 27..16 | 12 bit test pattern |
| 3 | ADC\_TEST\_PAT\_EN | R/W | 31 | Enable TEST mode |
| 4 | LATCH\_LOC\_0 | R/W | 7..0 | ADC data shift register data latch location |
| 5 | CLK\_select | R/W | 7..0 | ADC clock phase 0= 0 deg 1=90 deg 2=180 deg 3=270 deg |
| 6 | CHN\_select | R/W | 3..0 | ADC channel select |
| 6 | DATA MODE\_SEL | R/W | 4 | SET to read only one channel over UDP |
| 8 | WIB\_MODE | R/W | 0 | Set to enable WIB UDP MODE |
| 9 | ADC\_RD\_DISABLE | R/W | 0 | Set to disable readout 0 = running 1 = disabled |
| 10 | UDP\_FRAME\_SIZE | R/W | 11..0 | UDP FRAME SIZE NORMAL=0x1EE JUMBO FARME = 0xEFB |
| 16 | ANALOG\_SEL | R/W | 0 | DO NOT USE |
| 16 | JTAG\_SEL | R/W | 1 | DO NOT USE |
| 19 | FEMB\_TST\_MODE | R/W | 0 | DO NOT USE |
| 21 | INV\_RST | R/W | 0 | External clock RST invert |
| 21 | INV\_READ | R/W | 1 | External clock READ invert |
| 21 | INV\_IDXM | R/W | 2 | External clock IDXM invert |
| 21 | INV\_IDXL | R/W | 3 | External clock IDXL invert |
| 21 | INV\_IDL | R/W | 4 | External clock IDL invert |
| 21 | EXT\_CLK\_DIS | R/W | 5 | Disable external clocks |
| 22 | OFST\_RST | R/W | 15..0 | RST offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 23 | WDTH\_RST | R/W | 15..0 | RST width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 24 | OFST\_READ | R/W | 15..0 | READ offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 25 | WDTH\_READ | R/W | 15..0 | READ width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 26 | OFST\_IDXM | R/W | 15..0 | IDXM offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 27 | WDTH\_IDXM | R/W | 15..0 | IDXM width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 28 | OFST\_IDXL | R/W | 15..0 | IDXL offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 29 | WDTH\_IDXL | R/W | 15..0 | IDXL width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 30 | OFST\_IDL\_f1 | R/W | 15..0 | IDL1 offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 31 | WDTH\_IDL\_f1 | R/W | 15..0 | IDL1 width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 32 | OFST\_IDL\_f2 | R/W | 15..0 | IDL2 offset 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 33 | WDTH\_IDL\_f2 | R/W | 15..0 | IDL2 width 0=0ns 1=5ns 2= 10ns 3= 15ns |
| 34 | pll\_STEP0\_L | R/W | 15..0 | Phase control |
| 35 | pll\_STEP1\_L | R/W | 15..0 | Phase control |
| 36 | pll\_STEP2\_L | R/W | 15..0 | Phase control |
| 512-517 | SPI STRING WRITE LOCATION | R/W | 143..0 | SPI WRITE LOCATION |
| 592-597 | SPI STRING READ BACK LOCATION | R | 143..0 | SPI READBACK LOCATION |